

IRF1404

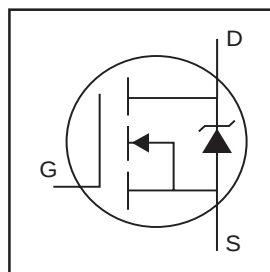
HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

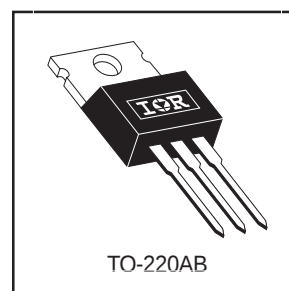
Description

Seventh Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



$V_{DSS} = 40V$
 $R_{DS(on)} = 0.004\Omega$
 $I_D = 162A\text{⑥}$



Absolute Maximum Ratings

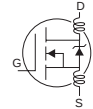
	Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	162⑥	A
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, V_{GS} @ 10V	115⑥	
I_{DM}	Pulsed Drain Current ①	650	
P_D @ $T_C = 25^\circ C$	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	2000	mJ
I_{AR}	Avalanche Current①	95	A
E_{AR}	Repetitive Avalanche Energy①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.0	V/ns
T_J	Operating Junction and	-40 to + 175	°C
T_{STG}	Storage Temperature Range	-55 to + 175	
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V$, $I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.036	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.0035	0.004	Ω	$V_{GS} = 10V$, $I_D = 95A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = 10V$, $I_D = 250\mu A$
g_{fs}	Forward Transconductance	106	—	—	S	$V_{DS} = 25V$, $I_D = 60A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	10	μA	$V_{DS} = 40V$, $V_{GS} = 0V$
		—	—	250		$V_{DS} = 32V$, $V_{GS} = 0V$, $T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	160	200	nC	$I_D = 95A$
Q_{gs}	Gate-to-Source Charge	—	35	—		$V_{DS} = 32V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	42	60		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	$V_{DD} = 20V$
t_r	Rise Time	—	140	—		$I_D = 95A$
$t_{d(off)}$	Turn-Off Delay Time	—	72	—		$R_G = 2.5\Omega$
t_f	Fall Time	—	26	—		$R_D = 0.21\Omega$ ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	7360	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1680	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	240	—		$f = 1.0MHz$, See Fig. 5
C_{oss}	Output Capacitance	—	6630	—		$V_{GS} = 0V$, $V_{DS} = 1.0V$, $f = 1.0MHz$
C_{oss}	Output Capacitance	—	1490	—		$V_{GS} = 0V$, $V_{DS} = 32V$, $f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance ⑤	—	1540	—		$V_{GS} = 0V$, $V_{DS} = 0V$ to $32V$



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	162	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	650		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$, $I_S = 95A$, $V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	71	110	ns	$T_J = 25^\circ\text{C}$, $I_F = 95A$
Q_{rr}	Reverse Recovery Charge	—	180	270	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.31mH$
 $R_G = 25\Omega$, $I_{AS} = 95A$. (See Figure 12)
- ③ $I_{SD} \leq 95A$, $di/dt \leq 150A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$

- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4

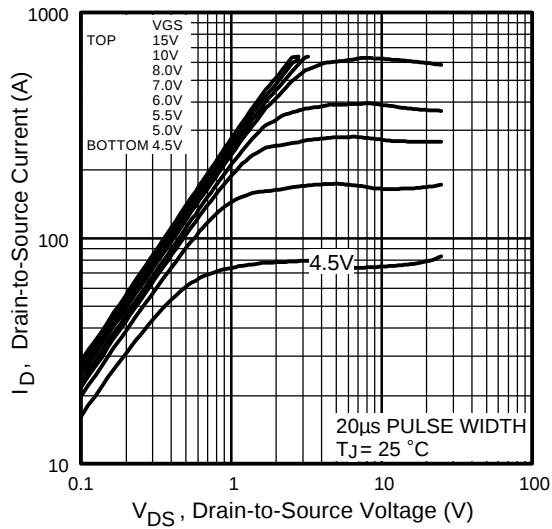


Fig 1. Typical Output Characteristics

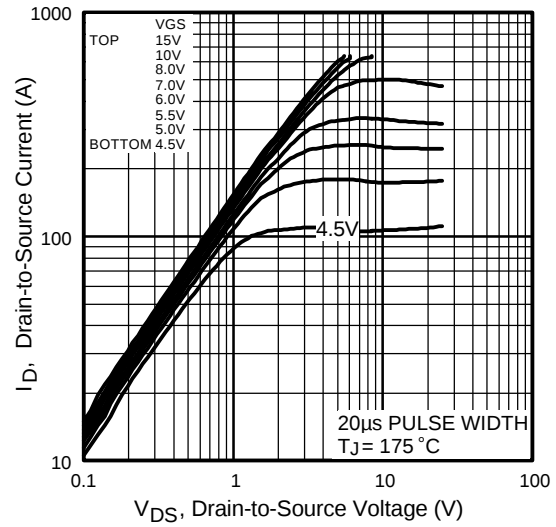


Fig 2. Typical Output Characteristics

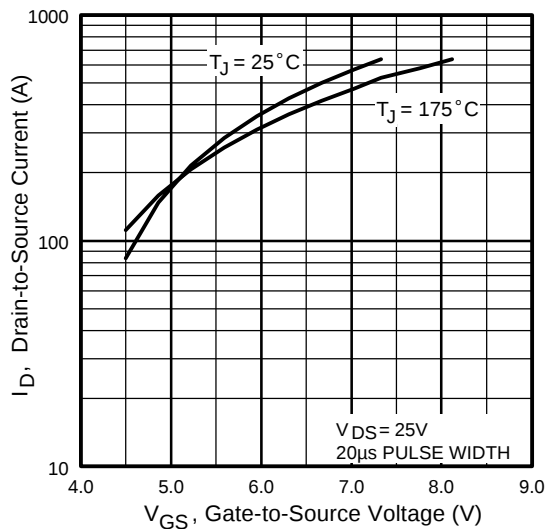


Fig 3. Typical Transfer Characteristics

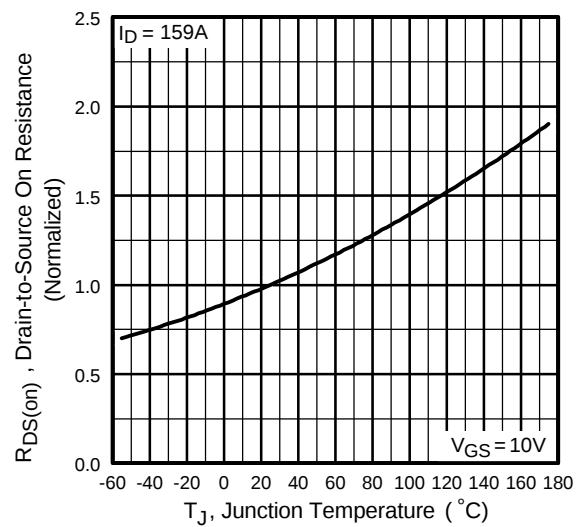


Fig 4. Normalized On-Resistance Vs. Temperature

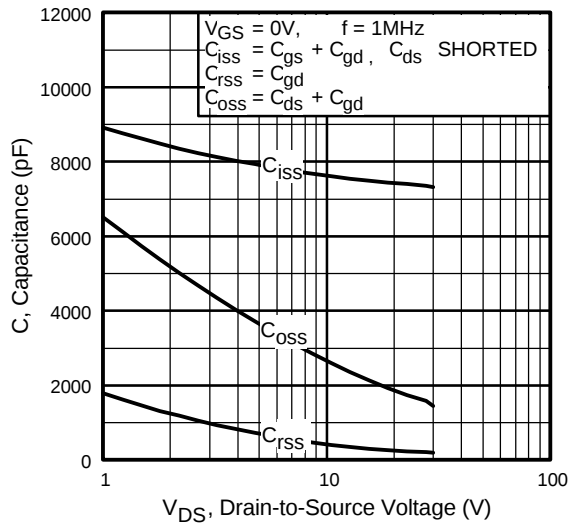


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

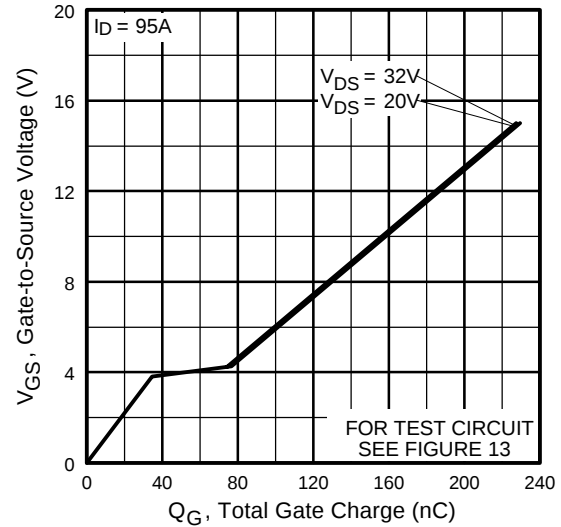


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

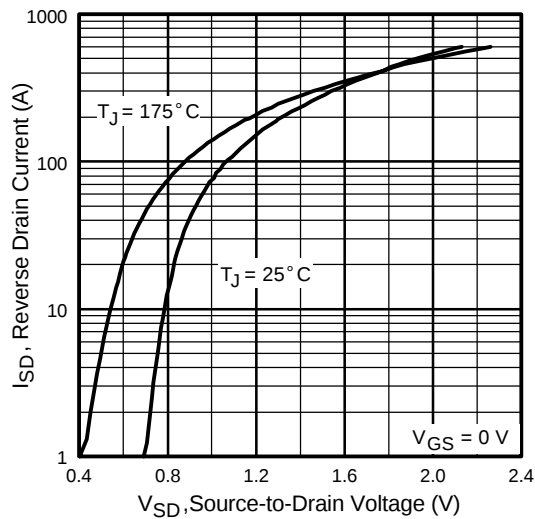


Fig 7. Typical Source-Drain Diode Forward Voltage

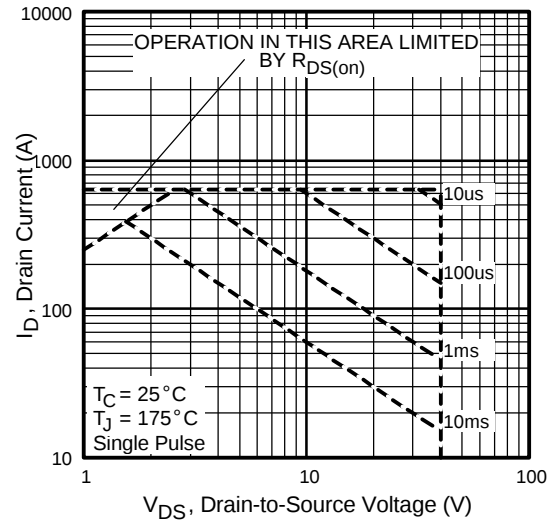


Fig 8. Maximum Safe Operating Area

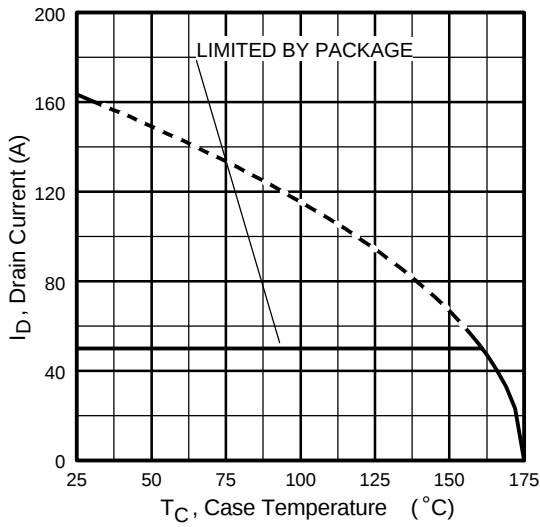


Fig 9. Maximum Drain Current Vs. Case Temperature

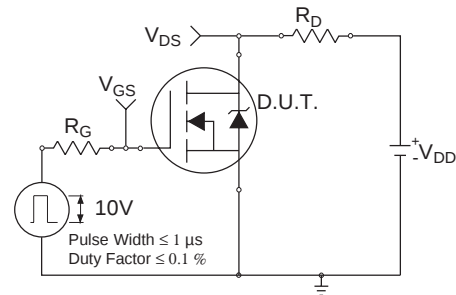


Fig 10a. Switching Time Test Circuit

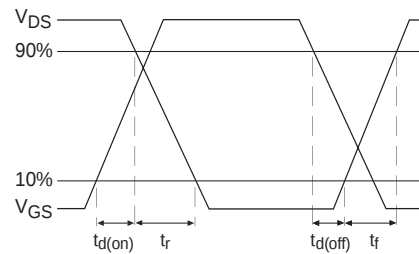


Fig 10b. Switching Time Waveforms

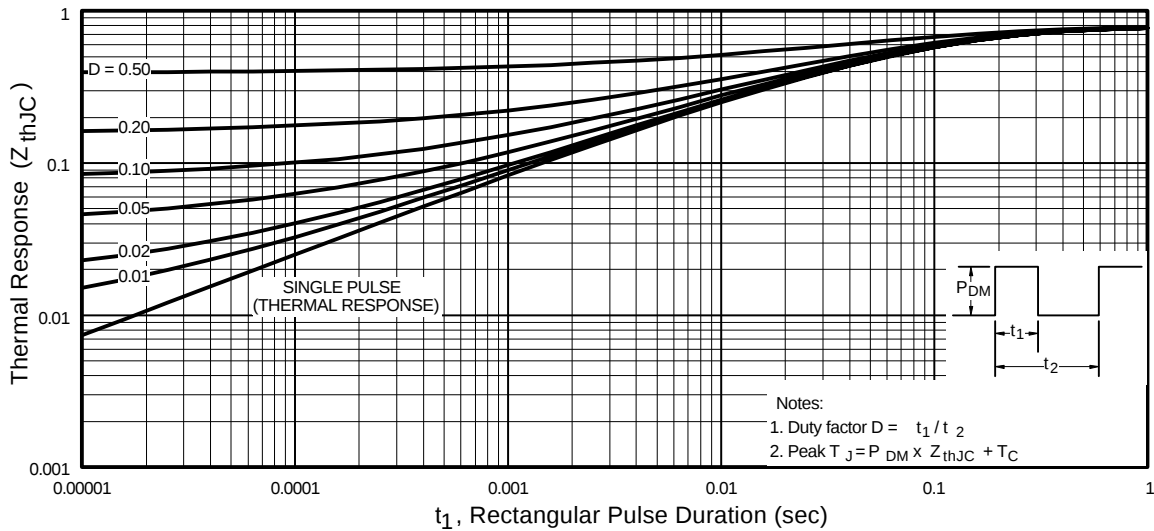


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

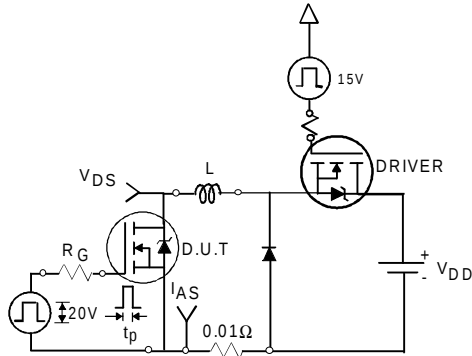


Fig 12a. Unclamped Inductive Test Circuit

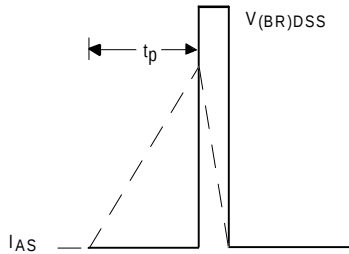


Fig 12b. Unclamped Inductive Waveforms

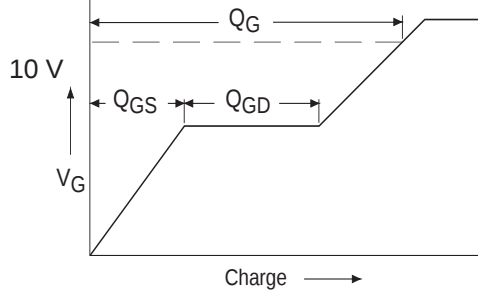


Fig 13a. Basic Gate Charge Waveform

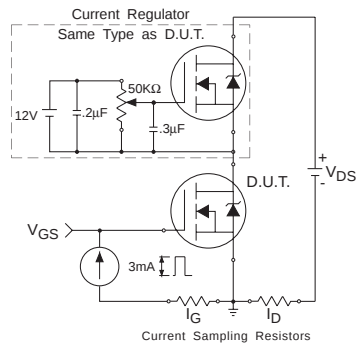


Fig 13b. Gate Charge Test Circuit

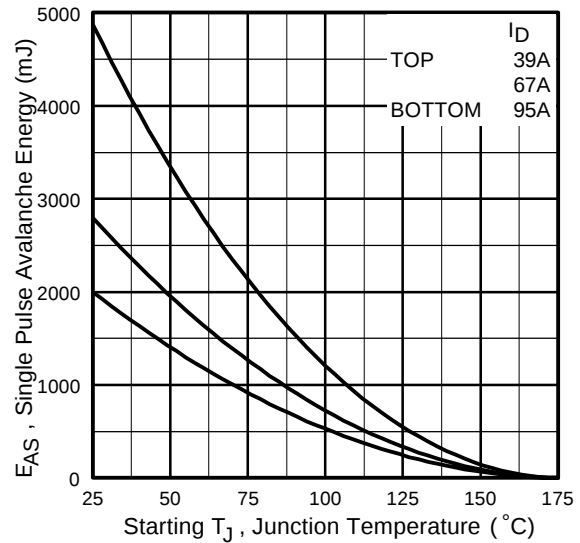


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

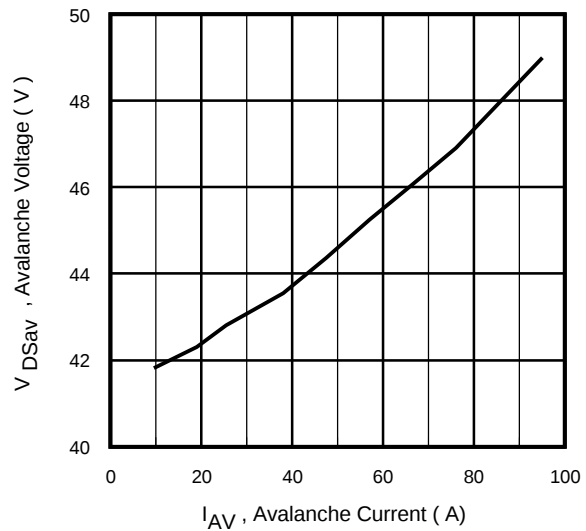
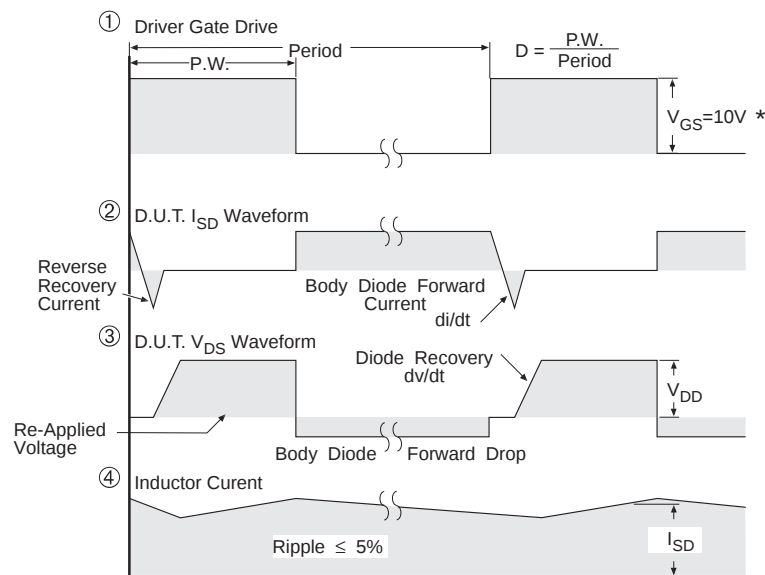
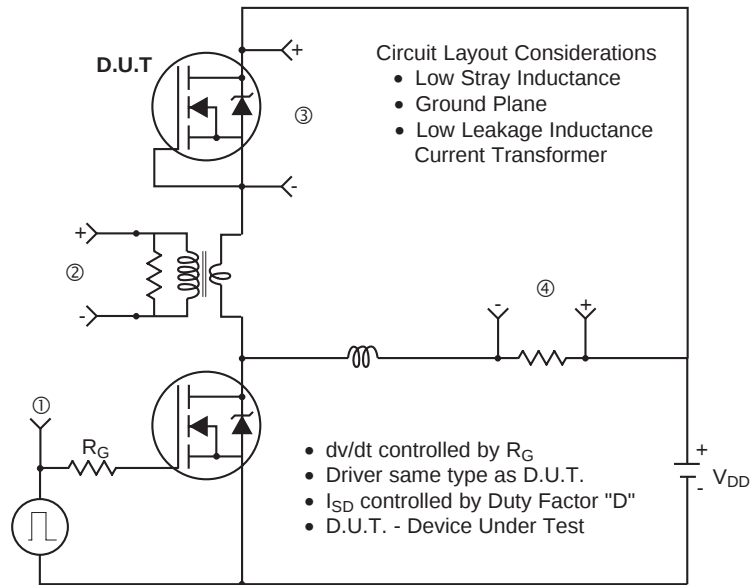


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

